Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original). A method for calibrating interface devices, which comprises the steps of:

a) providing a plurality of semiconductor devices each having the interface devices, a calibration unit connected to the interface devices, a calibration connection, a calibration path connected to the calibration connection, and a switching unit disposed in the calibration path for controlling and switching the calibration path;

b) generating, in a first semiconductor device of the semiconductor device, an active calibration signal connecting the calibration unit to the calibration connection using the switching unit;

c) calibrating the interface devices in the first semiconductor device;

d) generating a passive calibration signal isolating the calibration unit from the calibration connection using the switching unit; and

e) repeating steps b), c) and d) for all further semiconductor devices of the semiconductor devices.

Claim 2 (original). The calibration method according to claim 1, wherein the repeating step comprises repeating cyclically the steps b) through e).

Claim 3 (original). The calibration method according to claim 1, which further comprises:

providing each of the semiconductor devices with an instruction evaluation unit being connected to control and address connections on a respective semiconductor device, the control and address connections being provided for connecting to a control and address bus; and

generating the active calibration signal in the instruction evaluation unit on a basis of a calibration instruction transmitted via the control and address bus.

Claim 4 (original). The calibration method according to claim 3, which further comprises:

connecting the instruction evaluation unit to at least one respective data connection for connecting to a data line; and

generating the active calibration signal on a basis of a data signal transmitted via the data line.

Claim 5 (currently amended). The calibration method according to claim ~~1~~ 4, which further comprises forming the semiconductor devices as memory chips having a double data rate interface.

Claim 6 (original). The calibration method according to claim 1, which further comprises using the interface devices as output drivers for outputting data signals on data signal lines and/or terminations for low-reflection termination of the data signal lines.

Claim 7 (currently amended). The calibration method according to claim 1, wherein the repeating step comprises repeating the steps b) through e) [.] as a reaction to an operating condition in one of the semiconductor devices.

Claim 8 (original). A method for operating a plurality of semiconductor devices each connected to a common calibration reference and disposed to form a data bus system having a control and address bus and an at least partially common data bus, which comprises the steps of:

transmitting, in each case individually, calibration instructions to the semiconductor devices over the control and address bus in indirect or direct succession cyclically and/or on a basis of operating states of the data bus system;

connecting a calibration connection to a calibration unit in a respectively addressed semiconductor device;

calibrating interface devices in the respectively addressed semiconductor device using the calibration unit; and

switching the calibration connection to a high impedance state after completing a calibration process.

Claim 9 (original). The operating method according to claim 8, which further comprises addressing a semiconductor device for calibration on a basis of a data signal transmitted via at least one further data line.

Claim 10 (original). A semiconductor device, comprising:

control and address connections for connecting to a control and address bus;

data connections for connecting to a data bus;

a calibration connection for connecting to a calibration reference;

an instruction evaluation unit connected to said control and address connections;

a calibration path;

a calibration unit connected to said calibration connection through said calibration path;

a calibration signal path; and

a switching unit integrated in said calibration path for opening and closing said calibration path, said switching unit coupled to said instruction evaluation unit through said calibration signal path, said instruction evaluation unit

controlling said switching unit on a basis of calibration instructions transmitted via the control and address bus.

Claim 11 (original). The semiconductor device according to claim 10, wherein said switching unit is controlled on a basis of a data signal transmitted via at least one data line.

Claim 12 (original). The semiconductor device according to claim 10, wherein the semiconductor device is a memory chip and has a double data rate interface.

Claim 13 (original). The semiconductor device according to claim 10, further comprising output drivers which can be calibrated using the calibration reference for outputting data signals on data signal lines and/or calibratable terminations for terminating the data signal lines.

Claim 14 (original). A memory module for computer systems, comprising:

a plurality of semiconductor devices, each of said semiconductor devices containing:

control and address connections for connecting to a control and address bus;

data connections for connecting to a data bus;

a calibration connection for connecting to a calibration reference;

an instruction evaluation unit connected to said control and address connections;

a calibration path;

a calibration unit connected to said calibration connection through said calibration path;

a calibration signal path; and

a switching unit integrated in said calibration path for opening and closing said calibration path, said switching unit coupled to said instruction evaluation unit through said calibration signal path, said instruction evaluation unit controlling said switching unit on a basis of calibration instructions transmitted via the control and address bus.